

Fig. 1, eDRAM Cache Interface Circuits

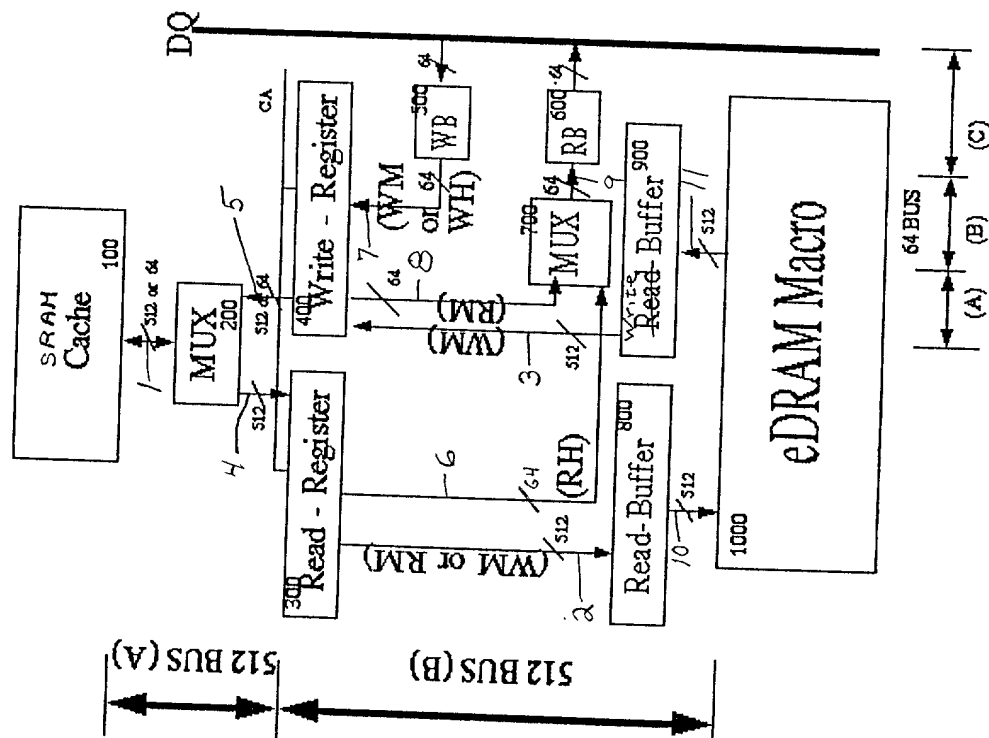


Fig. 2, Two-Cycle Read Hit Data Path

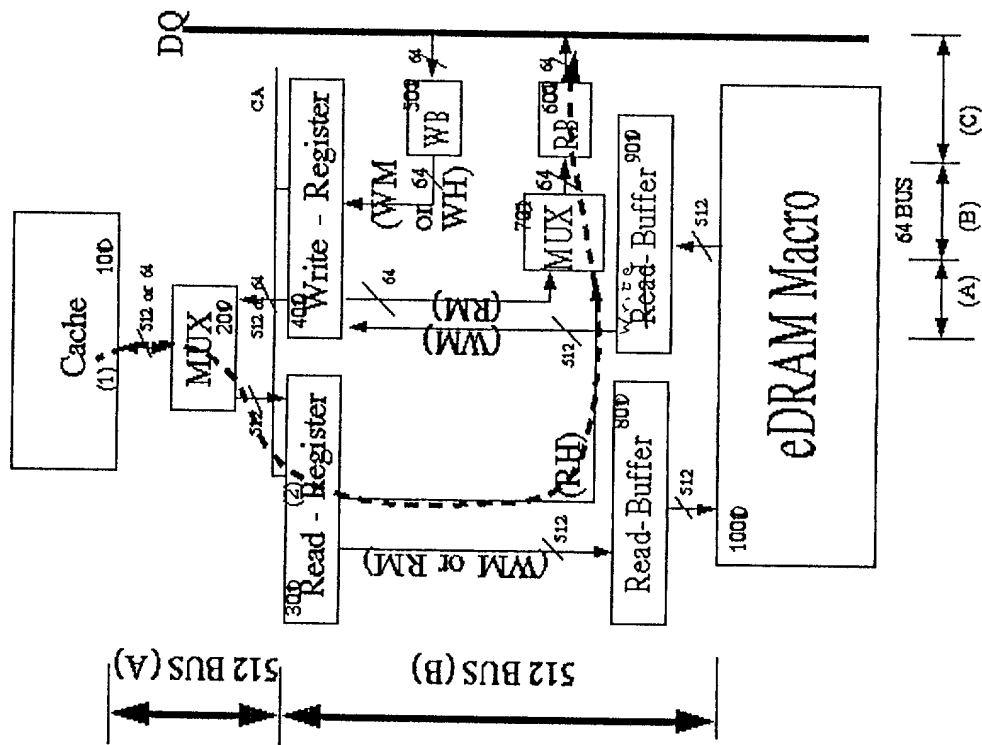


Fig. 5, Three-Cycle Write Miss Data Path

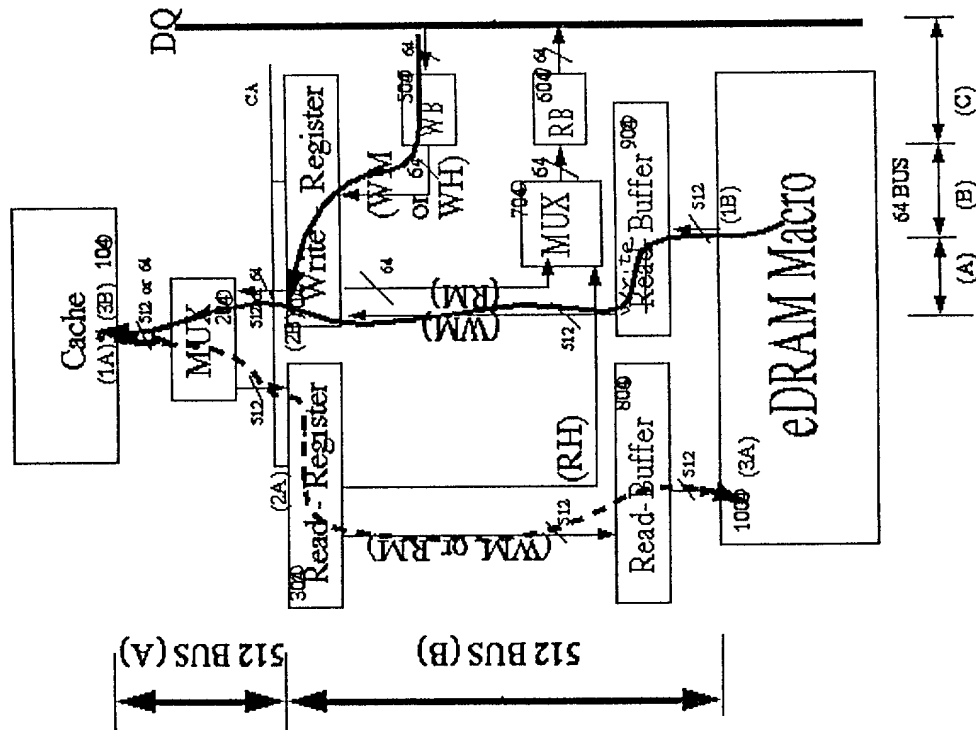


Fig-6, Pipe Operation Code:

| A1 | B1 | C1 | D1 | E1 | F1 |
|--------------|---------------|----------|------------|----------|----|
| Cache Decode | Cache Sig-Dev | Cache SA | Cache Cell | Read Reg | DO |

| A2 | B2 | C2 | D2 | E2 | F2 |
|-------------|--------------|---------|-----------|-----------|----|
| DRAM Decode | DRAM Sig-Dev | DRAM SA | DRAM Cell | Write Reg | DI |

Fig-7, Read/Write Pipeline Sequences.

| | | | | | |
|-----|----|----|----|----|----|
| RH: | A1 | B1 | C1 | E1 | F1 |
|-----|----|----|----|----|----|

| | | | | |
|-----|----|----|----|----|
| WH: | F2 | E2 | A1 | D1 |
|-----|----|----|----|----|

| | | | | | |
|-----|----|----|----|----|----|
| RM: | A1 | B1 | C1 | E1 | D2 |
| | A2 | B2 | C2 | E2 | A1 |
| | | | | | D1 |
| | | | | F1 | |

| | | | | | | |
|-----|----|----|----|----|----|----|
| WM: | A1 | B1 | C1 | E1 | A2 | D2 |
| | A2 | B2 | C2 | E2 | A1 | D1 |
| | F2 | E2 | | | | |

Fig.8-1, Parallel RH and WH Operations:

| | | | | | |
|-----|----|----|----|----|----|
| RH: | A1 | B1 | C1 | E1 | F1 |
| WH: | F2 | E2 | A1 | D1 | |

Fig.8-2, Parallel WH and RM Operations:

| | | | | | |
|-----|----|----|----|----|----|
| WH: | F2 | E2 | A1 | D1 | |
| RM: | A1 | B1 | C1 | E1 | A2 |
| | A2 | B2 | C2 | E2 | A1 |
| | | | | | F1 |

Fig.8-3, Parallel RH and WM Operations:

| | | | | | | |
|-----|----|----|----|----|----|----|
| RH: | A1 | B1 | C1 | E1 | F1 | |
| WM: | A1 | B1 | C1 | E1 | A2 | D2 |
| | A2 | B2 | C2 | E2 | A1 | D1 |
| | | | | F2 | E2 | |

Fig.8-4, Parallel RM and WM Operation

| | | | | | | |
|-----|----|----|----|----|----|----|
| RM: | A1 | B1 | C1 | E1 | A2 | D2 |
| | A2 | B2 | C2 | E2 | A1 | D1 |
| | | | | | F1 | |
| WM: | A1 | B1 | C1 | E1 | A2 | D2 |
| | A2 | B2 | C2 | E2 | A1 | D1 |
| | | | | F2 | E2 | |

Fig.9, Possible Operation Sequence and Delay

| | RH | RM | WH | WM |
|----|----|----|----|----|
| RH | 2 | 2 | 0 | 2 |
| RM | 2 | 2 | 0 | 2 |
| WH | 0 | 0 | 2 | 0 |
| WM | 2 | 2 | 0 | 2 |

Pipe Delay